| | | |
|---|---|---|
| 8 | | 1 |
| 7 | | 1 |
| 6 | | 1 |
| 5 | | 1 |
| 4 | | 1 |
| 3 | | 1 |
| 2 | | 1 |
| 1 | | 1 |

| LIST<br>LIST<br>SHEET | STRAN<br>STRANA<br>PAGE | IZDAJA<br>IZDANJE<br>ISSUE | LIST<br>LIST<br>SHEET | STRAN<br>STRANA<br>PAGE | IZDAJA<br>IZDANJE<br>ISSUE | LIST<br>LIST<br>SHEET | STRAN<br>STRANA<br>PAGE | IZDAJA<br>IZDANJE<br>ISSUE |
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| | Priimek in ime | Podpis | Gradivo | Odstopi netol. mer | Toplotna obdelava | Površ. zaščita | Pripadnost |
|---|---|---|---|---|---|---|---|
| | | | | | | | TRIGLAV |
| Konstr. | Kovačevič | Marko | Izdaja 1 | | | | |
| Projekt. | Kovačevič | Marko | Znak | | | | |
| Pregled. | Rogač | MR | Št. obv. 11-017 | | | | |
| Števil. | J. Bojanič | | Datum 17.12.86 | | | | |
| Stand. | | | Podpis | | | | |

Iskra Delta
proizvodnja računalniških sistemov in inženiring, p.o.

Naziv: TESTING PROCEDURE

| List | Stran | J | K | Identifikacijska številka |
|---|---|---|---|---|
| 1 | | | | 33839044 |

Namembnost kopije

Arhiv

| Merilo | Sekcija | Namesto identifikacijske številke |
|---|---|---|
| | | 22067044 |



Obr. 40

VME CPU/286

# Testing procedure

## Contents

## 1. Optical control

Purpose of this testing procedure step is to verify properly component installation on the PCB board. Component installation on the PCB board (including pin orientation) is specified by installation chart .
This testing procedure step must also include jumper settings verification based on version on some integrated circuits which are installed on the PC board and target system configuration (or factory jumper settings).

Especially check next component pin orientation or proper installation:

- EPROM-s: IC28, IC29
  at the position IC28 must be installed LOW eprom
  at the position IC29 must be installed HIGH eprom

  in the case of 24 pin EPROMS they must be installed into sockets down justified (P1 conector in front of you).

  Keep in mind that EPROM-s pin 1 has different orientation than any other IC.

- PAL installation: check if properly generated PAL circuits was installed into right position as shown in installation chart

- Electrolitic capacitors (C3, C11) have right + pol orientation.

- Check if all resistors were installed and their values are right.

- Check if all resistor networks were installed and pin 1 has right orientation.

- Check if cristal oscilator 16 MHz (Q1) have right pin 1 orientation.

- By using ohmmeter check if power pins at connector P1 (A9, A32) are in short connection.

- Check all diodes (including LEDs) have right anode orientation.

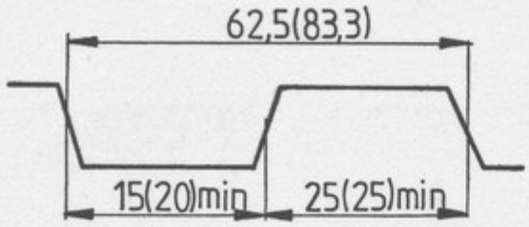
## 2. Power distribution control

- Check power pins at P1 (A9, A32) are not in short connection.
- Check all block capacitors are properly installed into PC board.
- Check IC11 have right anode (+) pin orientation.
- Check +12 V (P1, C31) power pin is not in short connection with GND (P1, A9), with -12V (P1, A31) or with +5V (P1, A32).
- Check -12V (P1, A31) power pin is not in short connection with GND (P1, A9) or with +5V (P1, A32).

## 3. Caracteristic signal forms and level check

This testing procedure phase must be done after power up. Purpose of this testing phase is to realize if the basic function of the board are operating properly like different clock generators CPU reset level, CPU status (running, halt ... ) and so on. All checks are made by using oscilograph and by monitoring status of LED diodes at the front panel. This testing phase must be done only by putting the VME CPU/286 into tested VME bus rack. JIACK jumper field must be connected as well as JBG jumper. All other jumper settings be done as defined for factory installation . Into EPROM sockets must be installed Debugger and self test EPROMs.

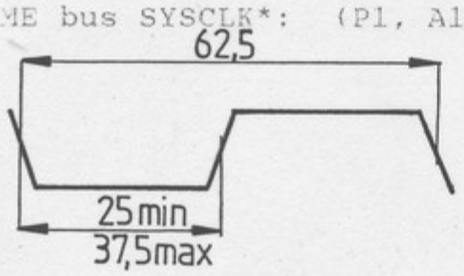
1. CPU 80286-16 CLK waveform: (IC2 pin 10)



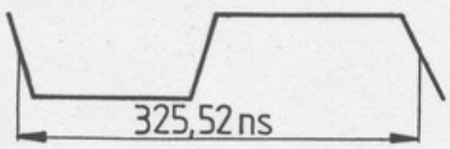

Rise & fall times max 10 ns for BR1 open or connected

(xx) value for BR1 connected

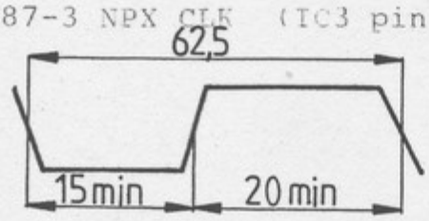
2. VME bus SYSCLK*: (P1, A10)




3. SCC PCLK (IC27 pin 20):

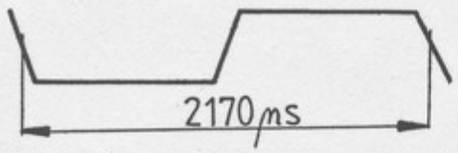



4. 80287-3 NPX CLK (IC3 pin 32):

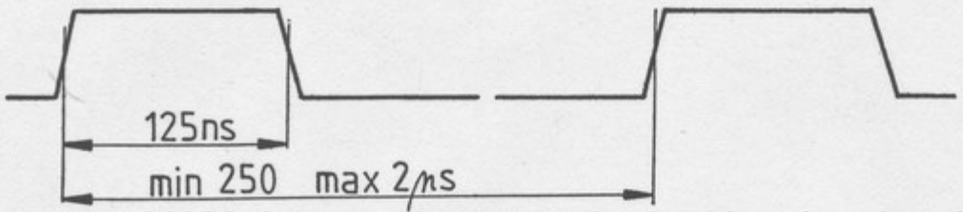



rise and fall times max 10 ns

5. Real Time Clock (IC26 pin 21)

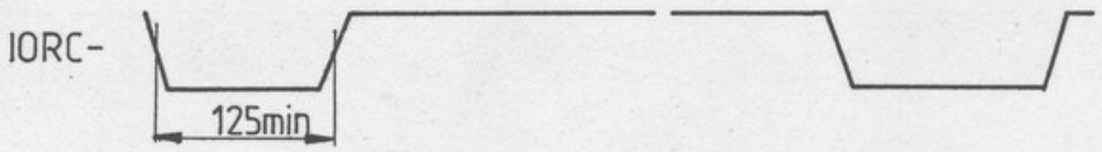



6. 82288-8 Local bus controller ALE (IC4 pin 5)




7. CPU 80286-8 Reset input (IC2 pin 12): low level
8. CENL (IC6 pin 16): low level

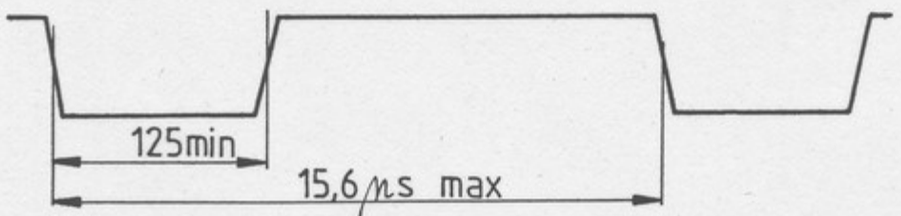
9. MRDC-, IORC- (IC4 pin 8/pin 12):





10. RPEA- (IC66 pin 3): high level

11. RAS- (IC88 pin 4):




12. MUX (IC68 pin 12): high level
13. BBS (IC13 pin 7): low level
14. BG3OUT* (IC56 pin 5): high level
15. LOCR (IC56 pin 12): low level
16. RPEB- (IC66 pin 6): high level
17. INTR (IC61 pin 17): low level
18. NMI (IC19 pin 8): low level
19. green LED: on
    yellow LED: off
    red LED: off

## 4. Self Test Procedure

After power up processor starts with Self Test Procedure. This procedure sequentially tests diferent functional submodules of the board. There are also test sequences for verificaton of properly VMEbus interface operatin for master and slave cycles. To start this test sequences processor checks if there are WDFD and DRAM-2 boards installed in the VME rack. If not VMEbus interface testing sequences are skipped.
For more detailed informations about Self Test Procedure see VME CPU/286 Software User's Manual.

## 5. Power and temperature range variation considerations

Maximum operating voltage and temperature range for VME CPU 286 board is specified (see VME CPU/286 specifications) as +5VDC +-5% and 0 - 55 C. Note that worst case analysis was done for temperature range 0 - 55 C. Exposure some IC parts (IC1, IC58) to absolute maximum rating conditions (0 - 55 C, 5VDC+- 5%) for extended periods may affect device reliability (iAPX 286/10 data sheet).
This must be take in count when testing the board or system with this board on maximum operating DC and temperature range.

## 6. Testing Equipment

Measurement equipment:

- 100 MHz graphoscope
- ohmmeter

Utility parts and equipment:

- tested VMEbus rack with power supply
- WDFD board
- DRAM board

- VT100 compatible terminal with cable
- VMEbus extender

Documentation

- VME CPU/286 Software User's Manual
- VME CPU/286 Hardware User's Manual